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CERTIFICATE OF TRANSMISSION

October 7, 2003

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Fax No.	:	703-872-9318
Attention	:	Examiner NADAV, ORI
Group Unit	:	2811
From	:	Jiawei Huang, Reg. No. 43,330
MESSAGE	:	Enclosed is an Amendment in 8 pages.

Sir:

I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office on **October 7, 2003** at the above indicated fax number.

Sign by: M. Chang
Michelle Chang

#25/F Amendt F
Y Robinson
10/15/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	
LIOU ET AL.	Examiner: NADAV, ORI
Serial No.: 09/467,675	Art Unit: 2811
Filed: 12/21/1999	Docket No.: 252103-4540
For: Structure for ESD Protection with Single Crystal Silicon Sided Junction Diode	

Entry
Adm 12/4/03

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-0710 (order No. JCLA5427).

RESPONSE TO OFFICE ACTION

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Office Action mailed August 11, 2003 has been carefully considered. In response thereto, please enter the following amendments and consider the following remarks.

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AMENDMENTS

1. (currently amended) An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

an input resistor including a plurality of single crystal Si resistors formed over an insulating material layer, electrically coupled between the input pad and the node, wherein the single crystal Si resistors are arranged in parallel connection; and

at least a single crystal silicon-sided junction diode formed over the insulating material layer, wherein the single crystal silicon-sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node.

2. (original) The structure according to claim 1, wherein the insulating material layer is made of oxide.

3. (original) The structure according to claim 1, wherein the insulating material layer includes a SOI.

4. (original) The structure according to claim 1, further comprising an input buffer electrically coupled between the node and the internal circuit.

5. (original) The structure according to claim 1, wherein the single crystal resistor is made of a single silicon layer on the insulating material layer.

6. (original) The structure according to claim 1, wherein the single crystal Si-sided junction diode includes a P/N junction formed on the insulating material layer.

7. (original) The structure according to claim 1, wherein the single crystal Si-sided junction diode includes a MOS transistor formed over the insulating material layer, and one of the source/drain region of the MOS electrically connects to a gate by a wiring line.

8. (original) The structure according to claim 1, wherein the single crystal Si-sided junction diodes comprises:

a first diode, electrically connected between the node and one terminal of a first power supply; and

a second diode, electrically connected between the node and one terminal of a second power supply.

cont F1

9. (currently amended) An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit formed from an insulating material layer on a SOI, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

an input resistor including a plurality of single resistors formed over the insulating material layer, wherein each of the single resistors is electrically coupled between the input pad and the node, and the single resistors are arranged in parallel connection; and

at least a single crystal sided junction diode formed over the insulating material layer, wherein the single crystal sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node.

10. (original) The structure according to claim 9, further comprising an input buffer electrically coupled between the node and the internal circuit.

11. (original) The structure according to claim 9, wherein each of the single crystal resistors is made from a single silicon layer on the insulating material layer.

12. (original) The structure according to claim 9, wherein the single crystal Si-sided junction diode includes a P/N junction formed on the insulating material layer.

13. (original) The structure according to claim 9, wherein the single crystal Si-sided junction diode includes a MOS transistor formed over the insulating material layer, and one of the source/drain region of the MOS electrically connects to a gate by a wiring line.

14. (currently amended) A semiconductor structure of ESD protection, the ESD protection electrically connects between an input pad and an integrated circuit, the semiconductor structure comprising:

a semiconductor substrate;

an insulating layer, formed on the semiconductor substrate;

an input resistor including a plurality of single crystal Si resistors, formed over the insulating layer, wherein the single crystal Si resistors are arranged in parallel connection;

at least a single crystal Si-sided junction diode formed over the insulating layer;

a first conductive layer, formed over the insulating layer, used to electrically connect one terminal of the input resistor and the input pad;

a second conductive layer, formed over the insulating layer, used to electrically connect another terminal of the input resistor and the integrated circuit; and

a third conductive layer, formed over the insulating layer, used to connect the single crystal Si-sided junction diode and the integrated circuit.

15. (previously presented) The structure according to claim 14, wherein each single crystal Si resistor includes a single crystal silicon layer.

16. (original) The structure according to claim 14, wherein the single crystal sided junction diode includes a single crystal silicon P/N junction.

Claims 17-18: (canceled)

19. (previously presented) The structure according to claim 14, wherein the single crystal Si resistors are isolated by an isolation structure.

20. (original) The structure according to claim 19, wherein the isolation structure includes a shallow trench isolation.

21. (currently amended) An ESD protection structure used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

an input resistor including a plurality of single crystal Si resistors formed on an insulating material layer, electrically coupled between the input pad and the node, wherein the single crystal Si resistors are arranged in parallel connection; and

a single crystal layer formed over the insulating material layer, wherein the single crystal layer comprises at least two doped regions with different dopant types to form a side junction diode, and the side junction diode is electrically coupled between one terminal of a corresponding power supply and a node.